

FIG. 1

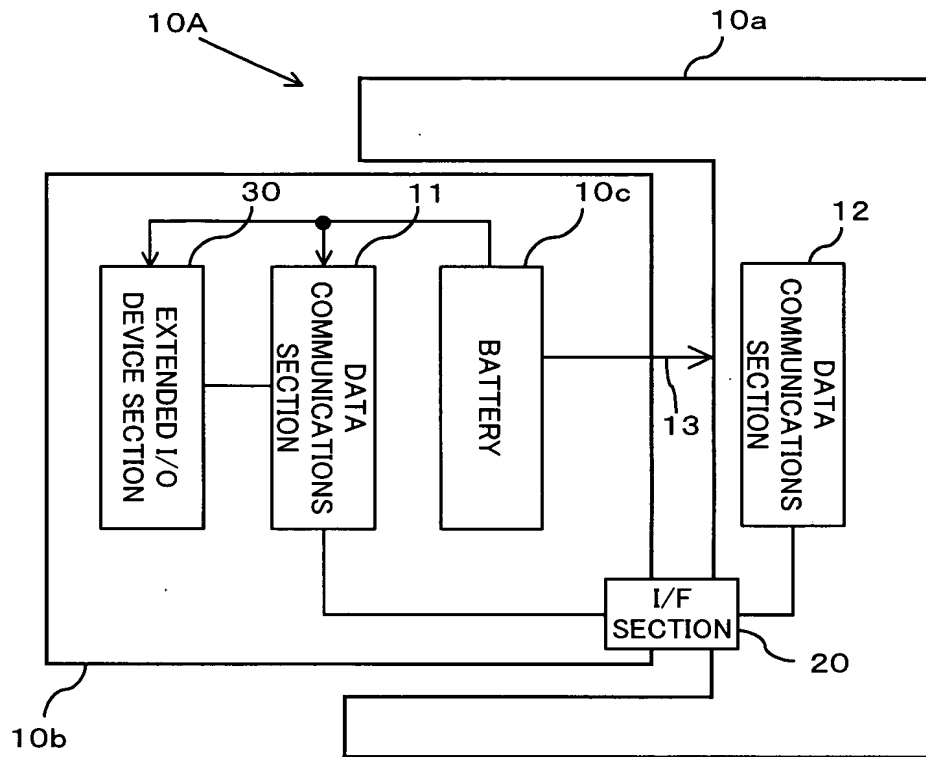


FIG. 1 is a block diagram of a system architecture. The system architecture includes a top section 10a, a bottom section 10b, and a middle section 10c. The top section 10a contains a DATA COMMUNICATIONS SECTION 12. The bottom section 10b contains an I/F SECTION 20. The middle section 10c contains an EXTENDED I/O DEVICE SECTION 30, a DATA COMMUNICATIONS SECTION 11, and a BATTERY 10c. The BATTERY 10c is connected to the DATA COMMUNICATIONS SECTION 11 and the I/F SECTION 20. The DATA COMMUNICATIONS SECTION 11 is connected to the EXTENDED I/O DEVICE SECTION 30 and the I/F SECTION 20. The I/F SECTION 20 is connected to the DATA COMMUNICATIONS SECTION 12 and the BATTERY 10c. A line 13 indicates a connection between the BATTERY 10c and the I/F SECTION 20. A line 30 indicates a connection between the EXTENDED I/O DEVICE SECTION 30 and the DATA COMMUNICATIONS SECTION 11.

FIG. 2

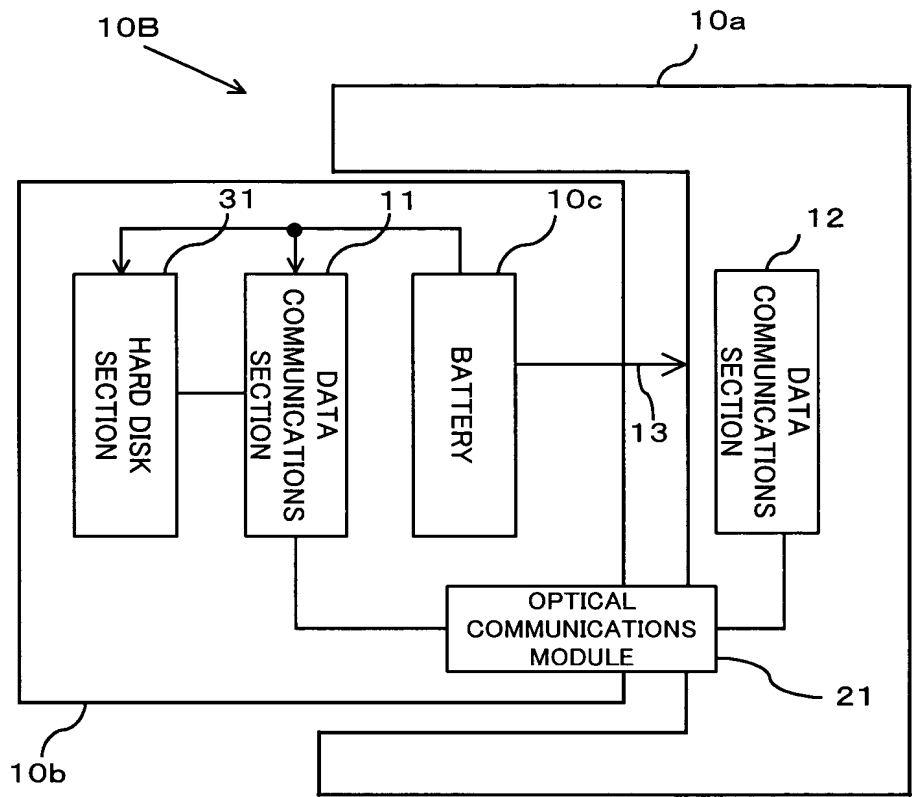


FIG. 2 is a block diagram of a system architecture. The system includes a HARD DISK SECTION, a DATA COMMUNICATIONS SECTION, a BATTERY, and an OPTICAL COMMUNICATIONS MODULE. The HARD DISK SECTION and the DATA COMMUNICATIONS SECTION are connected to a common data bus (11) via connection points (31). The BATTERY is also connected to the data bus (11). The DATA COMMUNICATIONS SECTION is connected to an external DATA COMMUNICATIONS SECTION (12) and an OPTICAL COMMUNICATIONS MODULE (21). The OPTICAL COMMUNICATIONS MODULE (21) is also connected to the external DATA COMMUNICATIONS SECTION (12). A connection (13) is shown between the BATTERY and the OPTICAL COMMUNICATIONS MODULE (21). The system is bounded by a top boundary (10a), a bottom boundary (10b), and a vertical boundary (10c).

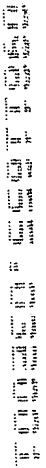


FIG. 4

FIG. 4

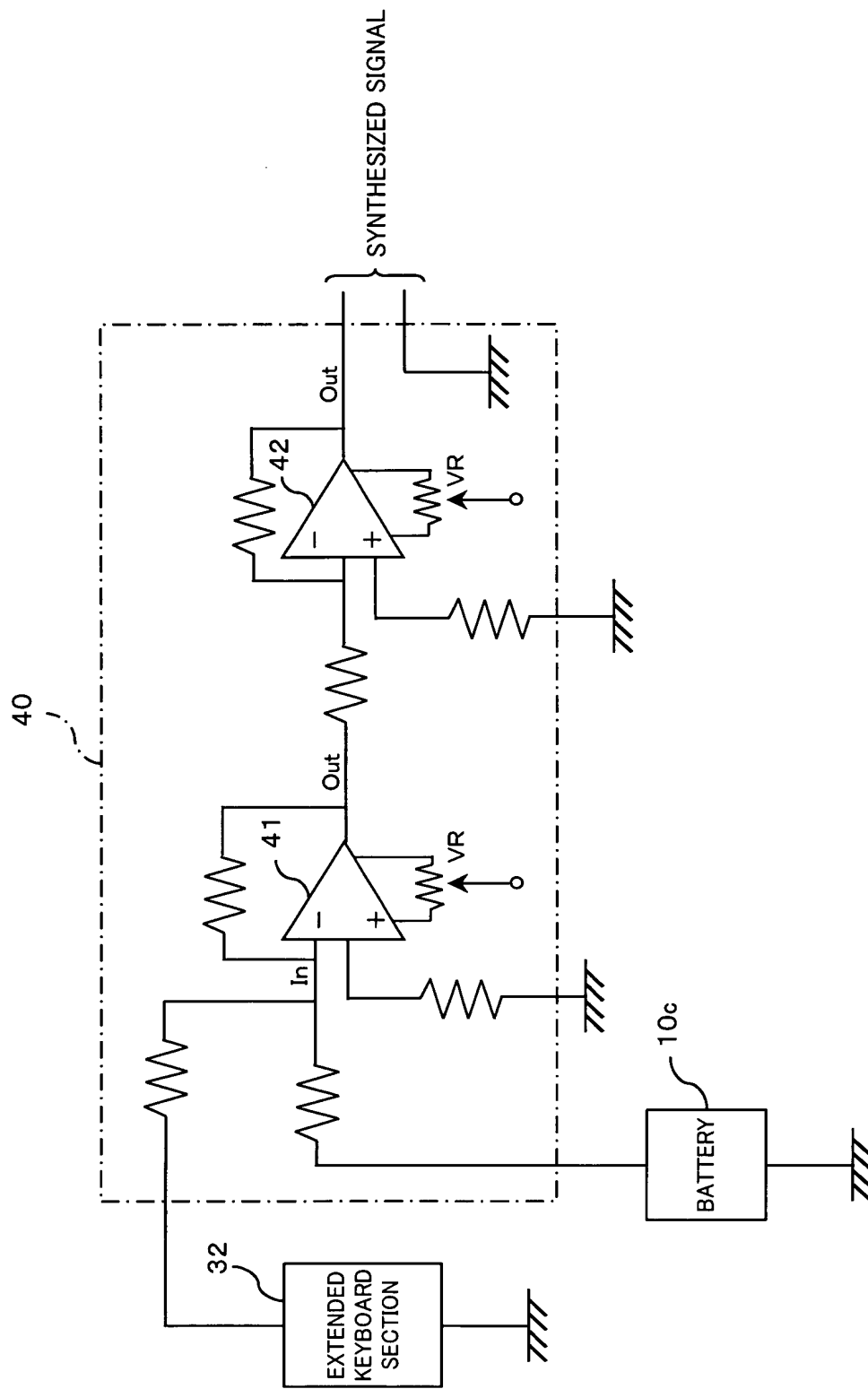


FIG. 5

FIG. 5

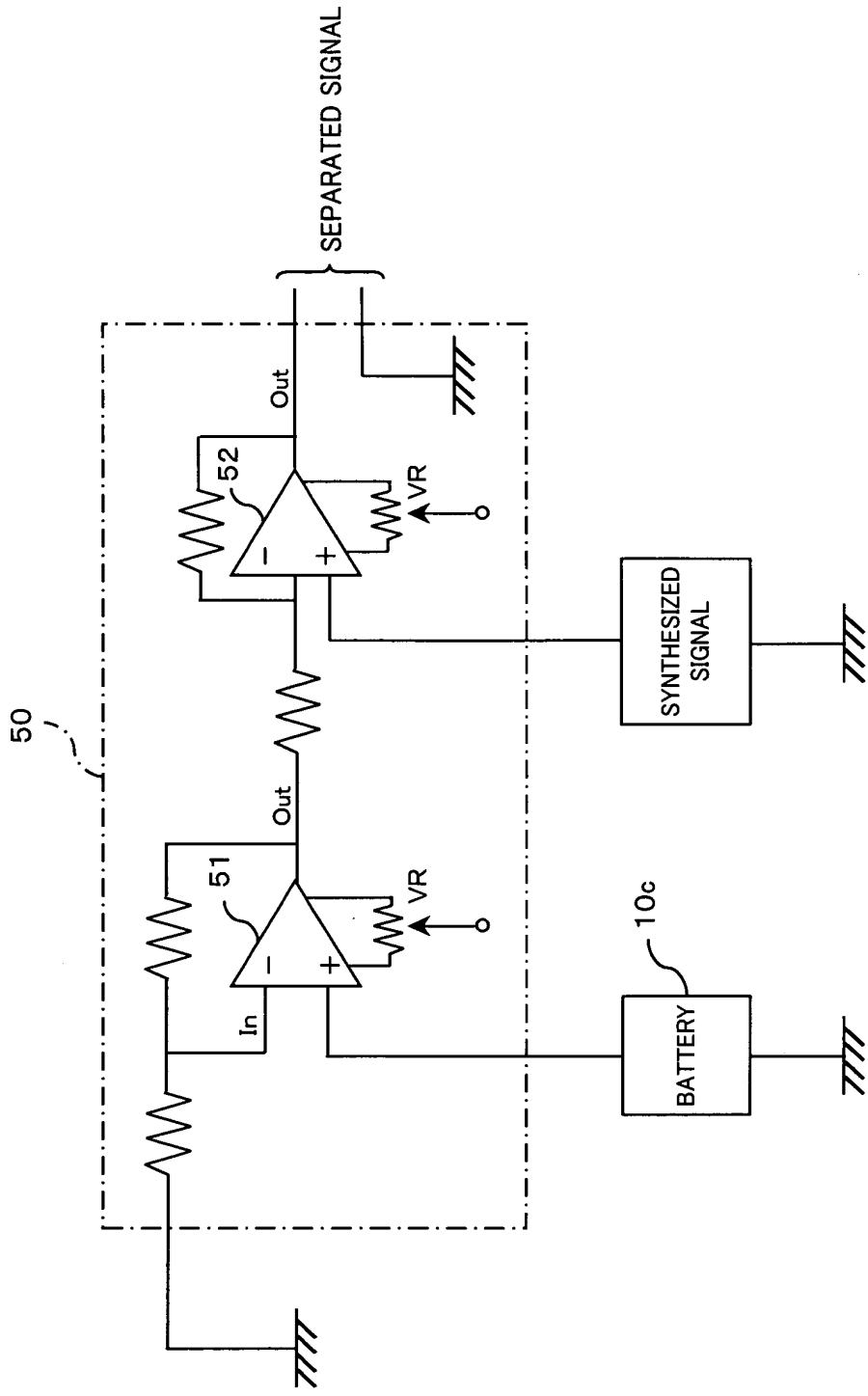


FIG. 6

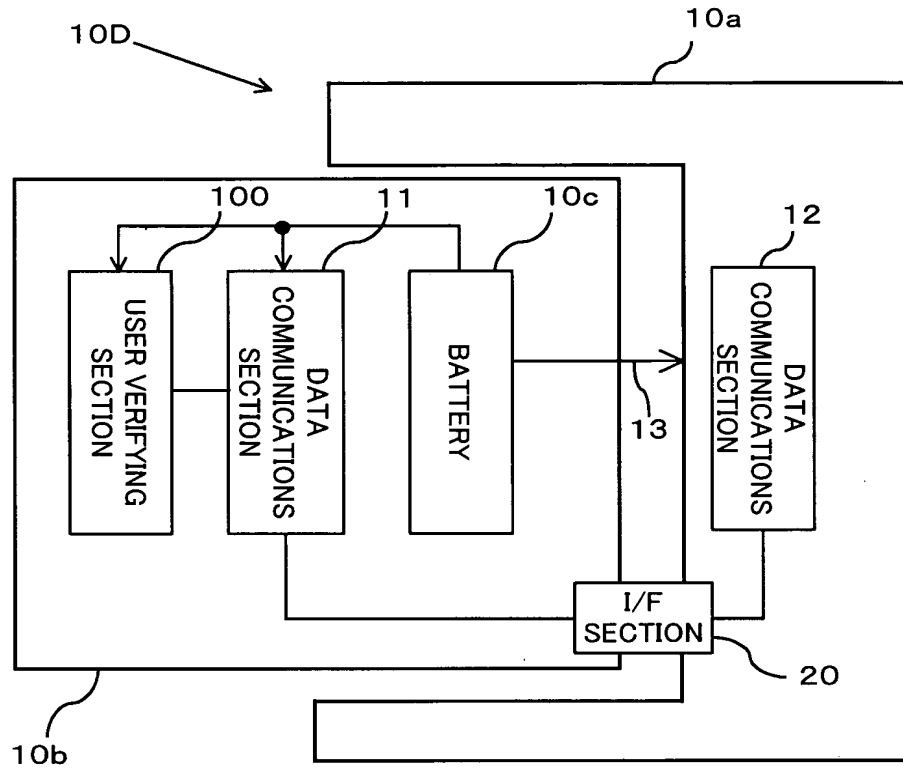


FIG. 7

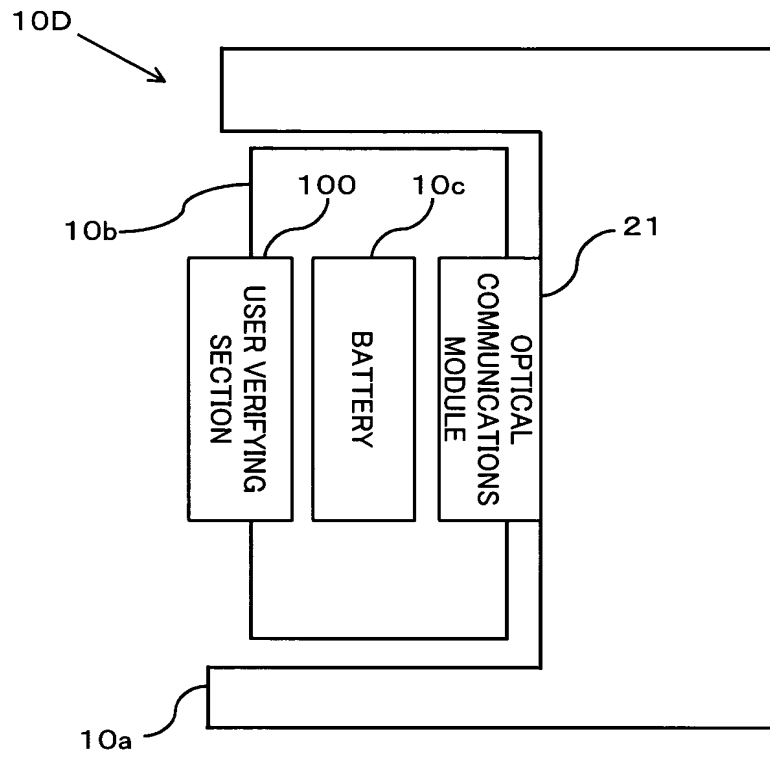


FIG. 7 is a block diagram of a device 100, which is part of a system 10D. The device 100 is shown as a rectangular block with three internal components: a USER VERIFYING SECTION, a BATTERY, and an OPTICAL COMMUNICATIONS MODULE. These components are arranged vertically within a larger housing 10D. The housing 10D is represented by a large rectangle with a notch on the left side, labeled 10a. The device 100 is labeled 10b. The components are labeled 100 (USER VERIFYING SECTION), 10c (BATTERY), and 21 (OPTICAL COMMUNICATIONS MODULE). The label 10D points to the housing, and 10a points to the notch. The label 10b points to the device 100, and 10c points to the BATTERY component. The label 21 points to the OPTICAL COMMUNICATIONS MODULE component.

FIG. 8

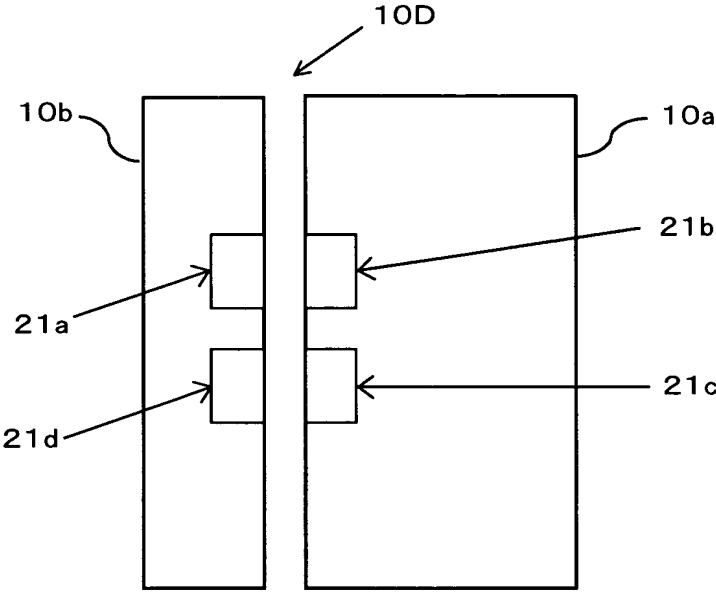


FIG. 9

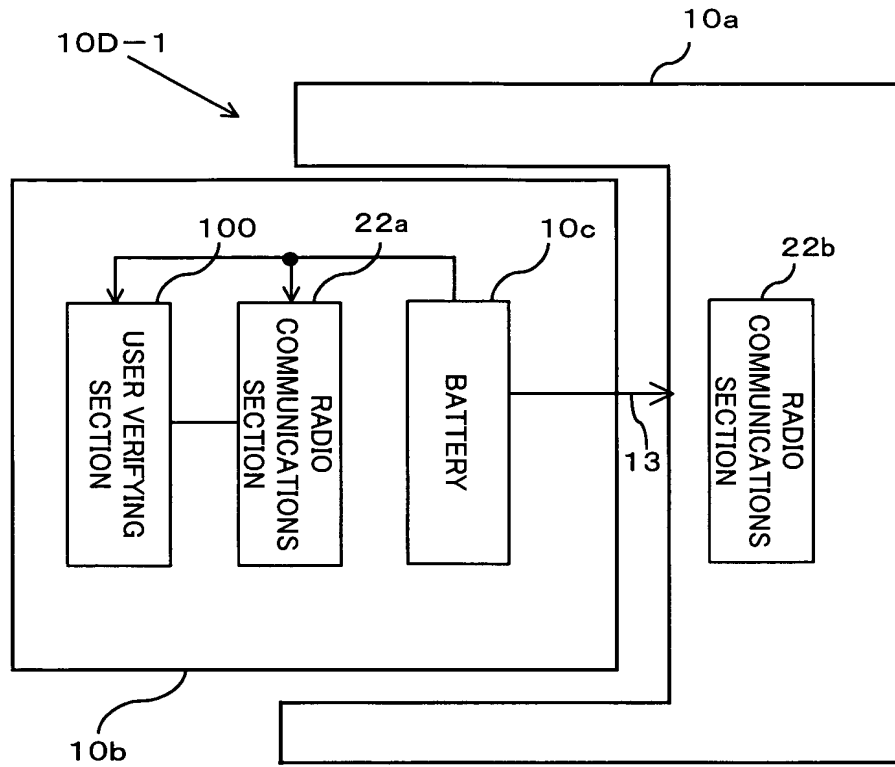


FIG. 9 is a block diagram of a device 10. The device 10 includes a sub-assembly 100. The sub-assembly 100 includes a user verifying section, a radio communications section, and a battery. The user verifying section, the radio communications section, and the battery are connected to a common bus line 22a. The battery is also connected to a line 10c. A switch 13 is connected to line 10c. The switch 13 is connected to a radio communications section 22b. The sub-assembly 100 is connected to the top edge of the device 10 via a line 10a. The bottom edge of the device 10 is labeled 10b.

FIG. 10

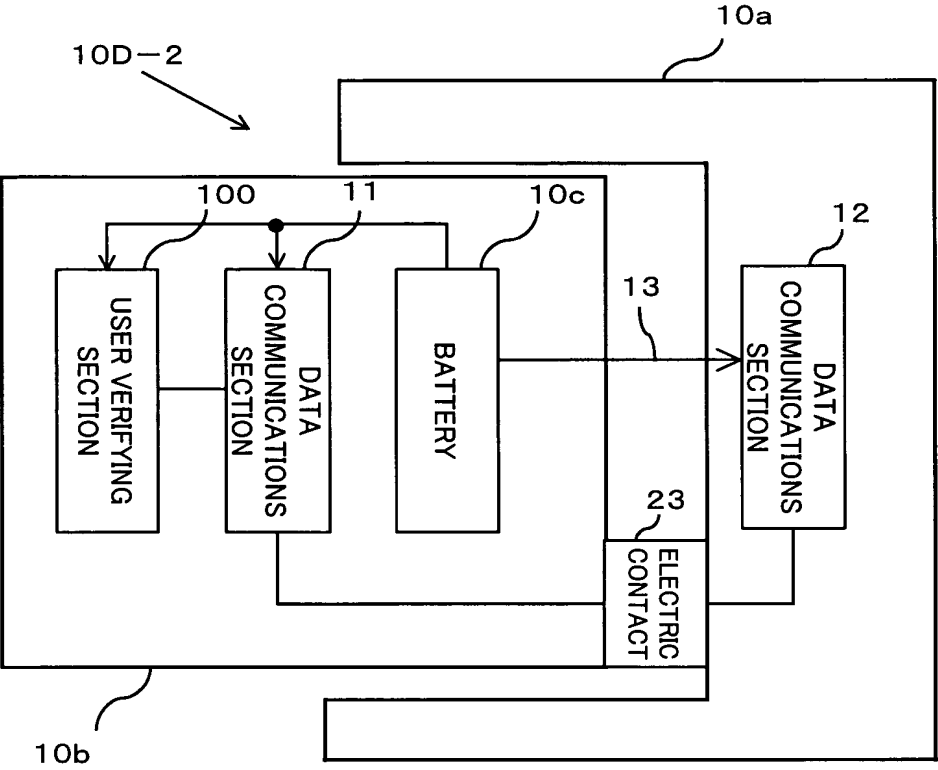


FIG. 10 is a block diagram of a device 10D-2. The device 10D-2 includes a top edge 10a and a bottom edge 10b. The device 10D-2 includes a central section 10c. The device 10D-2 includes a data communications section 12. The data communications section 12 is connected to a line 13. The line 13 passes through the central section 10c and is connected to an electric contact 23. The device 10D-2 includes a user verifying section, a data communications section, and a battery. The user verifying section is connected to the data communications section via a line 100. The battery is connected to the data communications section via a line 11. The data communications section is connected to the electric contact 23.

FIG. 11

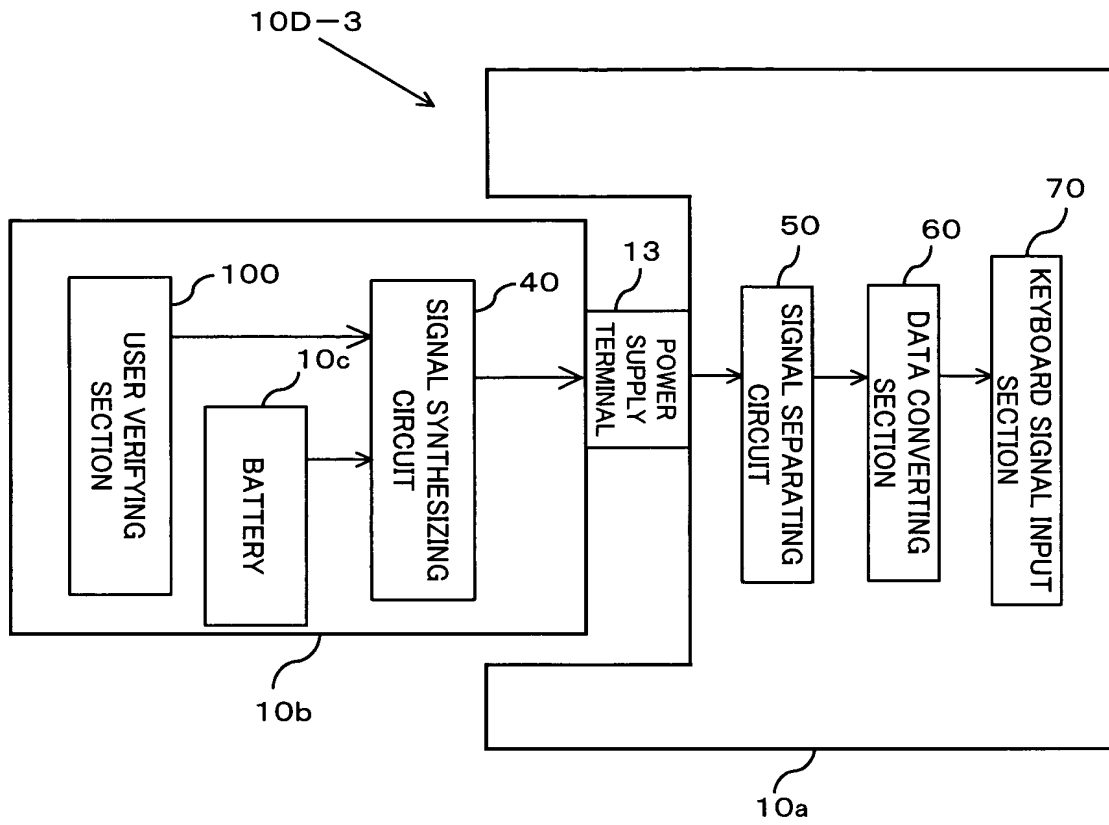


FIG. 12

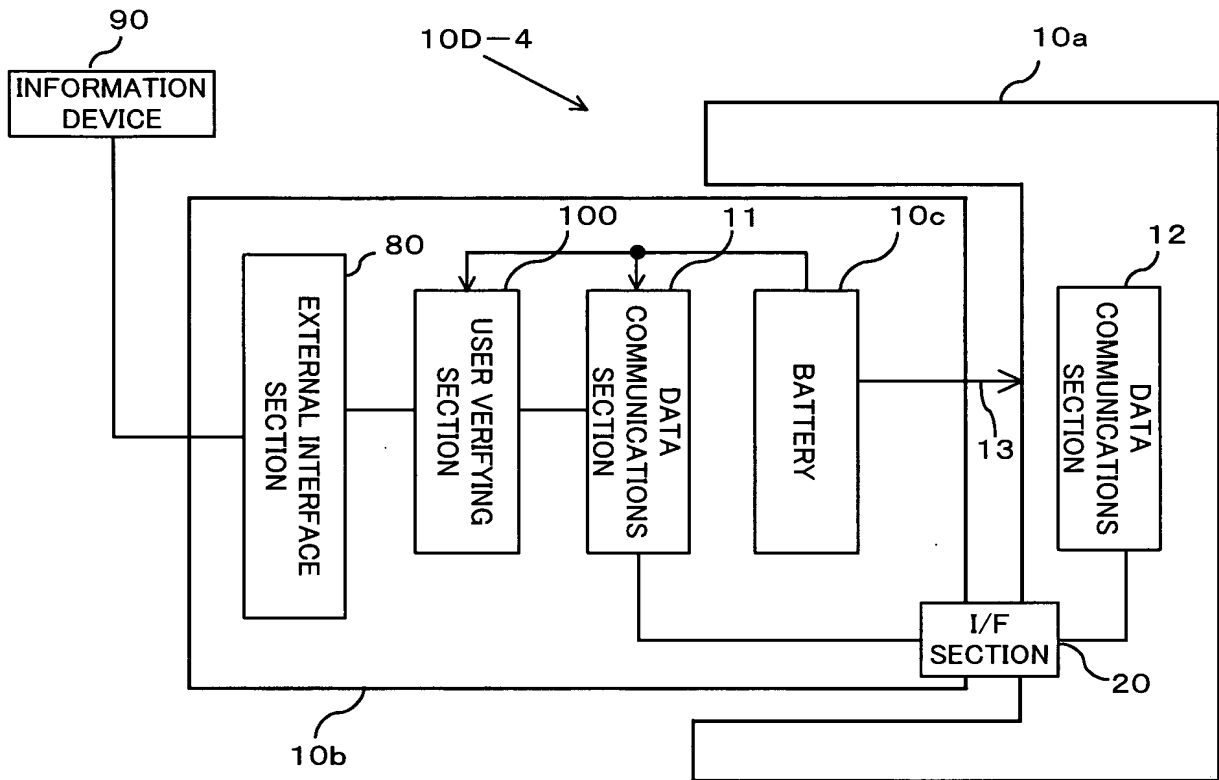


FIG. 13

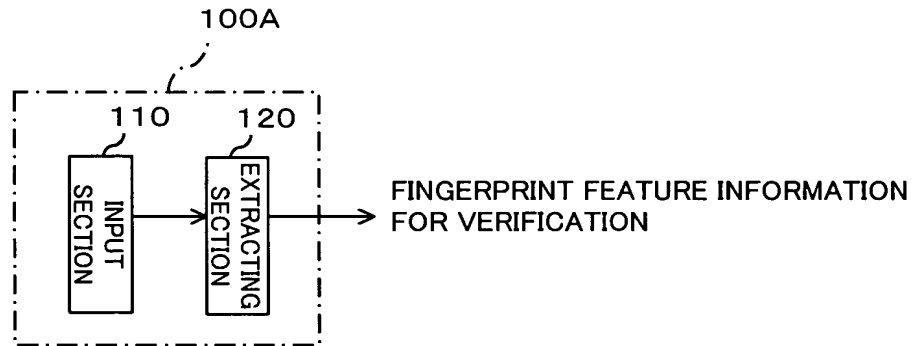


FIG. 14

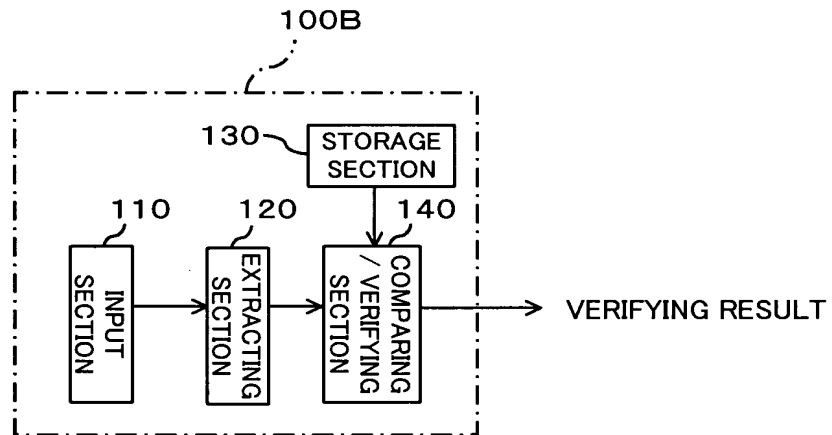


FIG. 15

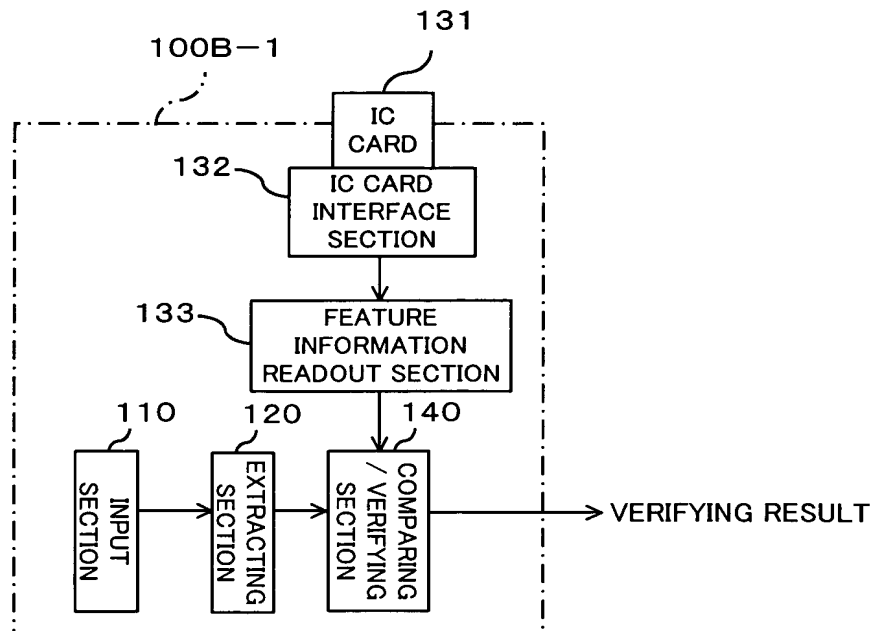


FIG. 16

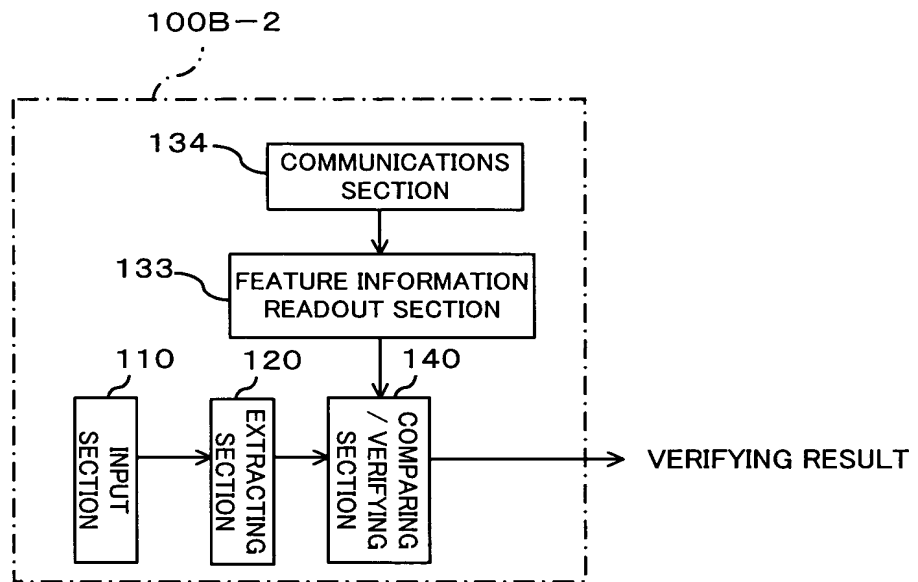


FIG. 17

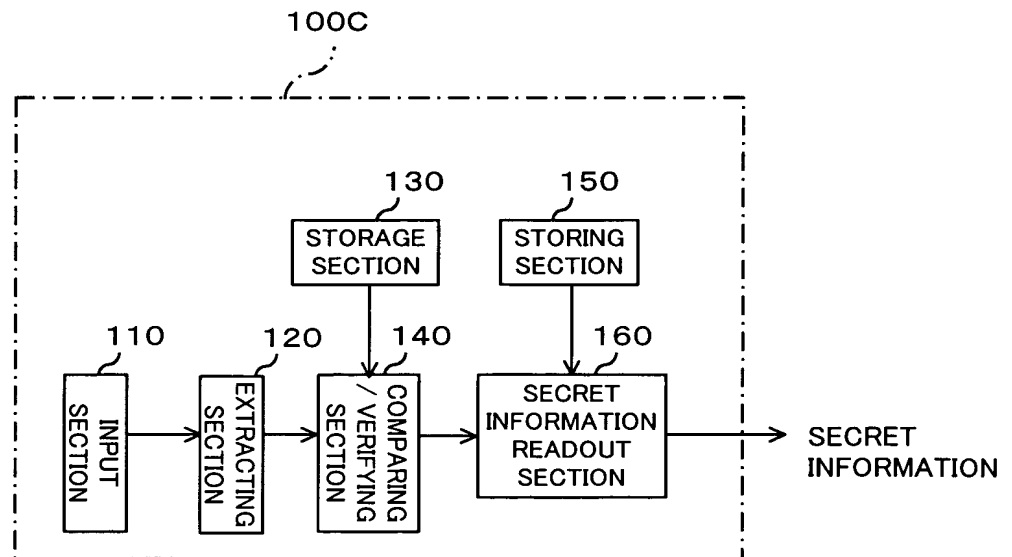


FIG. 18

